



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO 0037 VA	5927
23368 7590 09/18/2008 DINSMORE & SHOHL LLP ONE DAYTON CENTRE, ONE SOUTH MAIN STREET SUITE 1300 DAYTON, OH 45402-2023				
EXAMINER KIM, JAY C				
ART UNIT		PAPER NUMBER		
2815				
MAIL DATE		DELIVERY MODE		
09/18/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/605,293

Applicant(s)

CHAPEK, DAVID L.

Examiner

JAY C. KIM

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-12 and 14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-12 and 14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the Amendment filed June 23, 2008.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-12 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 9-12, the limitation "has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process" renders the claim indefinite. The metes and bounds of the claim are indefinite because the ordinary artisan would not know what level of metal contaminants is required to meet the limitation. Whether or not metal contaminants are "sputtered", metal contaminants make no structural difference in the product. Further, whether or not the metal contaminants come from a Kauffman ion implantation process or another source also does not make a structural difference in the product. Considering metal contaminants can come from many different sources (including subsequent metallization processes), there is no way to determine if metal contaminants in the final product came from the Kauffman ion implantation process or another source. The level of sputtered metal contaminants resulting from a Kauffman ion implantation process can vary due to varying process conditions such as

implantation time and energy. The amount of metal contaminants from other sources may also vary depending on manufacturing techniques used to make the device. The specification provides no guidance as to the amount of metal contaminants that can be imparted when using a Kauffman ion implantation process, nor does the specification provide any guidance as to the amount of metal contaminants imparted when using the disclosed plasma source ion implantation process. Further, when looking at a final (or intermediate) product, there is no way for the ordinary artisan to determine whether or not any metal contaminants existing in the silicon dioxide layer are from a Kauffman ion implantation process, or from another source. Therefore, the ordinary artisan would not be able to determine the level of metal contaminants covered by the scope of the claim. In view of all of the above noted considerations, the limitation does not particularly point out and distinctly claim the level of metal contaminants in the product.

Regarding claim 14, the limitation "a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass" renders the claim indefinite. The listed materials are insulating materials. It is unclear how the substrate can be a semiconductor substrate when it is made of an insulating material.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 9 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (hereinafter the APA).

Regarding claim 9, as best the Examiner can ascertain the claimed invention, the APA anticipates the claim. The APA discloses, on page 1 lines 12-16, a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the layer of silicon dioxide, the layer of polycrystalline silicon having a smooth morphology. The APA discloses the layer of silicon dioxide having been doped with hydrogen ions. The APA is considered to inherently teach a substrate as the APA teaches DRAM's and DRAM's inherently have a substrate. Though the APA does not explicitly state a layer of polysilicon is on the layer of silicon dioxide, it is implicitly understood that the polysilicon is formed seeing that the APA discusses performing the hydrogen doping of the layer of silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The APA does not explicitly state the layer of silicon dioxide "has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process", but this limitation is inherent. The level of metal contaminants imparted by the Kauffman ion implantation process of the APA can be considered "reduced" compared

to an arbitrary ion implantation process conducted at a higher energy and/or for a longer time. Regardless of the particular parameters of the APA process, there can always be another Kauffman ion implantation process that is conducted at a higher temperature or for a longer time period. In other words, since the claim does not specify the particular conditions of the Kauffman ion implantation process, there can always be some Kauffman ion implantation process that imparts more metal contaminants than that of the APA process.

5. Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al. (US 5,946,585), as evidence by Nakanishi et al. (US 6,265,247).

Regarding claims 9 and 10, Figure 1D of Zhang discloses a semiconductor substrate (101) (col. 4, lines 14-16), a layer of silicon dioxide (104) (col. 4, lines 48-49) formed on the semiconductor substrate (101), the silicon dioxide layer inherently containing hydrogen, and a layer of polycrystalline silicon (105) (col. 4, lines 56-58) formed on the layer of silicon dioxide, the layer of polycrystalline silicon (105) having a smooth morphology (at least to some degree), and a gate oxide formed on the substrate from the layer of silicon dioxide. Zhang discloses the silicon dioxide layer (104) is formed by plasma CVD (col. 4, lines 44-46). Therefore, the layer inherently contains at least some hydrogen. Nakanishi discloses that a silicon oxide film formed by plasma CVD contains hydrogen (col. 2, lines 30-34). The limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process" is merely a product-by-process limitation that does not structurally distinguish the claimed invention

over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966. Since no Kauffman ion implantation process is conducted during the manufacturing of the device of Zhang, it is inherent that the oxide layer has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process.

6. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Shufflebotham (US 5,711,998).

As best the Examiner can ascertain the claimed invention, Figure 3 of Shufflebotham discloses a thin film transistor comprising a semiconductor substrate (301) formed from glass (col. 5, lines 13-15), a layer of polycrystalline silicon (306A/307/306B) (col. 5, lines 18-20) formed on at least a portion of the semiconductor substrate, the layer of polycrystalline silicon having a smooth morphology (any layer can be considered smooth to at least some degree), a layer of an insulating material (308) formed on at least a portion of the layer of polycrystalline silicon, a gate oxide (308) (col. 5, lines 17-18) formed from the layer of insulating material, a source region and a drain region formed in the layer of polycrystalline silicon, and a gate electrode (304) formed on the insulating material. Shufflebotham discloses performing a hydrogenation process in which hydrogen ions diffuse into the polycrystalline silicon layer (see col. 6,

lines 17-49, for example). In this process, it is inherent that at least some hydrogen ions reach the substrate. The limitation "implanted therein by plasma source ion implantation" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by- process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966. Note that Shufflebotham does not use a Kauffman ion implantation process. Therefore, as best the Examiner can ascertain the claimed invention, it is inherent that the substrate (301) has reduced sputtered metal contaminants in comparison with a semiconductor substrate doped with ions deposited by a Kauffman ion implantation process.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of the APA.

Regarding claim 10, Burns et al. teach a field effect transistor in Fig. 9.8. Burns et al. teach a substrate, a silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer, and a gate oxide, a source and a drain in the substrate where a gate electrode is formed from the layer of polycrystalline silicon.

Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or the silicon dioxide layer having reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process.

The APA teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. The APA as discussed above inherently teaches the silicon dioxide "has reduced sputter metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process". In the combination of the references, the gate oxide would be formed from the layer of silicon dioxide having hydrogen ions implanted therein.

Burns et al. and the APA are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with the APA to obtain the invention of claim 10.

Regarding claim 11, Burns et al. teach on pages 380-381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted therein.

Regarding claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (US 5,576,229) in view of the APA.

Murata et al. teach a thin film transistor (Fig. 6E) comprising a semiconductor substrate of glass, a layer of polycrystalline silicon (507) formed on a portion of the substrate, an insulating layer (503) formed on a portion of the polycrystalline silicon, a gate oxide, a source region (507a) and drain region (507b) formed in the polycrystalline silicon, and a gate electrode (504) formed on the insulating layer.

Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate having reduced sputtered metal contaminants in comparison with a substrate doped with ions deposited by a Kauffman ion implantation process.

The APA teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. The APA as discussed above inherently teaches the silicon dioxide "has reduced sputter metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process". Murata et al. and the APA are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film.

Therefore, it would have been obvious to combine Murata et al. with the APA to obtain the invention of claim 14.

Response to Arguments

10. Applicant's arguments filed June 23, 2008 have been fully considered but they are not persuasive.

Applicant argue that "there is no need to quantify or to determine the amount of metal contaminants as the claim clearly conveys that the claimed process produces fewer metal contaminants than a process utilizing the Kauffman ion implantation

technique". One of ordinary skill in the art cannot determine whether the amount of metal contaminants is smaller than that produced by a Kauffman ion implantation process without measuring the amount.

Applicant argues that "Applicant wishes to point out that such materials are commonly used as semiconductor substrates", that "as described and explained in the specification at page 7, lines 18-27, such materials are commonly used to form the substrate on which a semiconductor device is fabricated", and that "further, the recited materials find clear support in the specification as originally filed". Applicant does not specifically claim a substrate on which a semiconductor device is formed. Rather, Applicant claims a semiconductor substrate, which suggests that the substrate comprises semiconductor.

Applicant argues that "claim 9 does not refer to an "arbitrary" [sic] implantation process, but rather refers specifically to the comparison of a silicon dioxide layer deposited with ions by a plasma ion source implantation process with that of the (same) silicon dioxide layer deposited with ions by a Kauffman ion implantation process". Applicant does not claim specific operating parameters of "a Kauffman ion implantation process", and therefore one Kauffman ion implantation process would inherently produce reduced sputtered metal contaminants in comparison with another Kauffman ion implantation process. The Examiner has provided a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

Applicant argues that "hence the claimed comparison cannot be inherent in the APA", that "the APA is a Kauffman ion implantation process", and that "that process cannot result in reduced sputtered metal contaminants in comparison to itself". See the above response.

Applicant argues that "the method by which the layer has been formed directly affects the composition of the final product, e.g., with regard to the amount of metal contaminants in the silicon dioxide layer", and that "a silicon dioxide layer with no or a reduced amount of metal contaminants is compositionally different than a silicon dioxide layer with greater levels of metal contamination". Zhang et al. disclose that a silicon dioxide layer is formed by plasma CVD, and Applicant does not provide evidence that the plasma CVD process will always produce greater level of metal contamination in comparison with any Kauffman ion implantation process.

Applicant argues that "there is no teaching or suggestion in either Zhang et al. or Nakanishi et al. of doping a layer of silicon dioxide with hydrogen ions deposited by a plasma source implantation process". As stated in rejection of claim 9, the limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art.

Applicant argues that "the Examiner has concluded that such a layer would inherently contain some hydrogen; however, this conclusion is based on speculation, not facts or evidence". Nakanishi et al. clearly disclose a hydrogen ion concentration of a silicon oxide film formed by plasma CVD. The Examiner has provided a basis in fact

and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

Applicant argues that "the references are silent, and silence cannot provide the required factual basis for anticipation". See the above response.

Applicant argues that "there is absolutely no teaching or evidence that if hydrogen ions existed in the layer of Zhang, such ions would be located in the surface of such a layer as claimed". The surface of the layer of silicon dioxide is inherently doped with hydrogen ions, because the hydrogen ions are substantially uniformly distributed in the layer of silicon dioxide.

Applicant argues that "from this teaching, one skilled in the art would not conclude that Nakanishi et al. teach the claimed process in which a layer of silicon dioxide is doped with hydrogen ions formed by a plasma source ion implantation process, nor would one conclude from reading Nakanishi et al. that the claimed process results in reduced sputtered metal contaminants when compared with a layer of silicon dioxide doped with hydrogen ions deposited by a Kauffman ion implantation process". The limitation "having been doped with hydrogen ions deposited by a plasma source ion implantation process" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. Also, since no Kauffman ion implantation process is conducted during the manufacturing of the device of Zhang et al., it is inherent that the oxide layer has reduced sputtered metal contaminants in comparison with a layer of silicon dioxide doped with ions deposited by a Kauffman ion implantation process. Further, see the above response.

Applicant argues that "claim 14 is patentable over Shufflebotham for the same reasons discussed above". See the above response.

Applicant argues that "as pointed out above, the APA does not teach that a silicon dioxide layer deposited with ions by a plasma ion source implantation process compared with that of the (same) silicon dioxide layer deposited with ions by a Kauffman ion implantation process would have reduced metal contaminants". As stated above, Applicant does not claim specific operating parameters of "a Kauffman ion implantation process", and therefore one Kauffman ion implantation process would inherently produce reduced sputtered metal contaminants in comparison with another Kauffman ion implantation process. The Examiner has provided a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

Applicant argues that "claim 14 is patentable over the cited references for the same reasons discussed above". See the above response.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
September 13, 2008

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815

